

Digigital design lab

Exp 3: NAND, NOR, XOR Gates.





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**Experiment 3: NAND, NOR, XOR Gates**

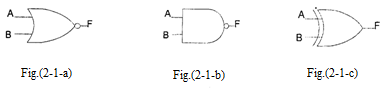
**Objective:** To study the ( NAND, AND, XOR) Gates .and to realize the Boolean equation for these Gates.

**Introduction:**

The symbol of a NOR gate is shown in Fig (2- l-a), and the Boolean expression for the NOR gate is F=; in de Morgan’s theorem, F=****=Ā.B.

The symbol of a NAND gate is shown in Fig.(2-1-b), and the Boolean expression for the NAND gate is F=**** in de Morgan’s theorem, F=****= .

The symbol of XOR gate is shown in fig(2-1-c), and the Boolean expression for the XOR gate is F== A.****+ Ā.B, you can see that **XOR** gate are construct from two AND gates & two NOT gates with one OR gate.



**Required Equipment:**

* KL-31001 Digital Logic Lab base unit
* Module KL-33002.

**Procedure:**

1. **Item(1) NOR Gate Characteristics Measurement (Module KL-33002 block a)**
2. Connect inputs(A, B) to Data Switches SW0, SW1 and output Fl to Logic Indicator L1. Set SW0 to “0”, observe states of Fl at SW1=”0” and SW1=” 1” .

**Does the circuit act as a NOT gate?**

1. Insert a connection clip between A and B, then connect A to SWO and Fl to L1. What is the state of Fl when SW0=0 and SW0=1 .

**Does the circuit act as a NOT gate?**

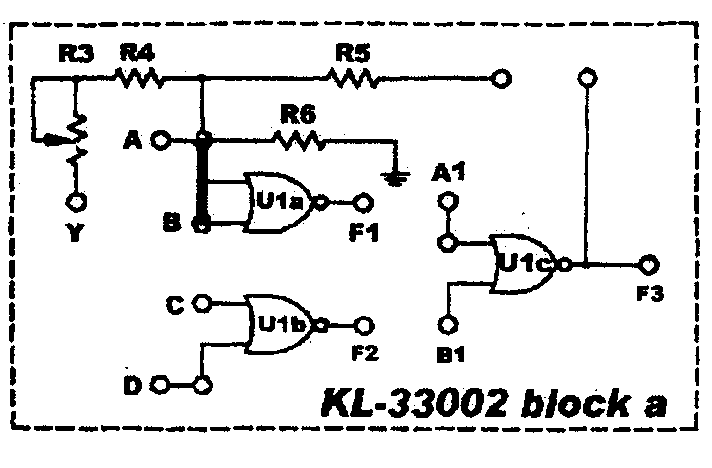


Fig.(2-2)

1. Insert Connection clips between (A, B), (Fl ,Al) and(Al, B1), then connect input A to SW0 and output F3 to L1. What is the state of F3 when SW0=0 and SW0=1?

**Does the circuit act as a buffer?**

1. Insert connection clips between (F1,A1) and (A1,B1). Connect inputs A to SW0, B to SW1; and output F3 to L1. Follow the input sequence and record the output states in table(2-1).

Table(2-1)

|  |  |  |
| --- | --- | --- |
| INPUT | | OUTPUT |
| SW1(B) | SW0(A) | F3 |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

1. Insert Connection clips (according to figure below), and connect A to SW0, D to SW1, F3 to L1, then follow the input sequence and record the output F3 in table(2-2).

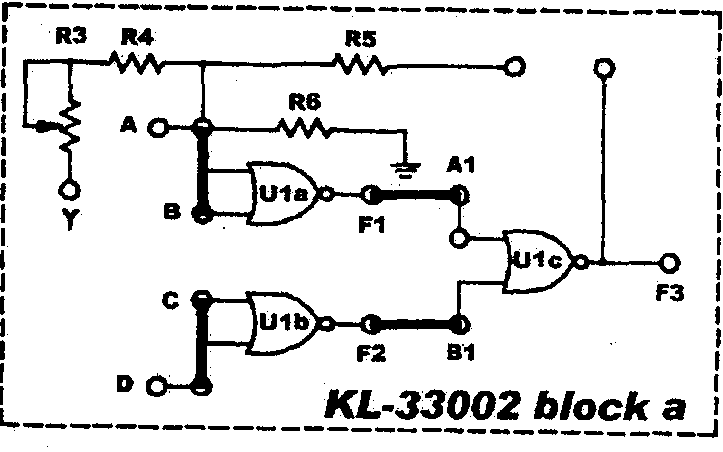


Fig.(2-3)

Table (2-2).

|  |  |  |
| --- | --- | --- |
| INPUT | | OUTPUT |
| SW1(D) | SW0(A) | F3 |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

1. **Item 2: NAND Gate Characteristics Measurement (Module KL-33002 block b)**
2. Connect B to SWo, C to SWl, F1 to L5 , then follow the input sequence and record the output F1 in table(2-3).

Table(2-3)

|  |  |  |
| --- | --- | --- |
| INPUT | | OUTPUT |
| SW1(B) | SW0(C) | F1 |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

1. Insert Connection clips (according to figure below), and connect A to SW0, D to SW1 and F4 to L1, then follow the input sequence and record the output F4 in table (2-4).

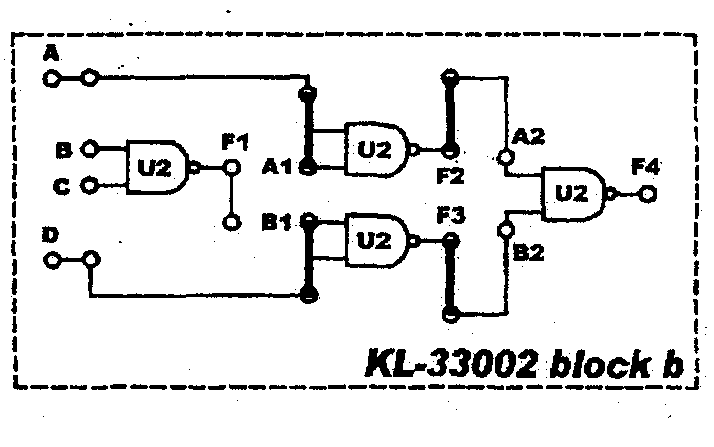


Fig.(2-4)

|  |  |  |
| --- | --- | --- |
| INPUT | | OUTPUT |
| SW1(D) | SW0(A) | F4 |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

Table (2-4).

1. **Item 3: XOR Gate Characteristics Measurement (Module KL-33002 block c)**
2. Insert connection clips between (A1,F7) and (F6,B1) according to figure(2-5).
3. Connect A to SW0, B to SW1 and F5 to L5, then follow the input sequence and record the output F5 in table(2-5).

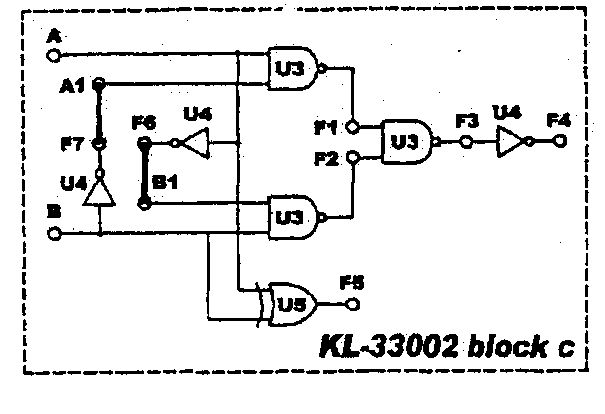


Fig.(2-5)

Table (2-5)

|  |  |  |
| --- | --- | --- |
| INPUT | | OUTPUT |
| SW1(B) | SW0(A) | F5 |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

1. Insert connection clips between (A,B), (C,D), (F1,A1), (F1,B1), (F2,A2) and (F3,B2) according to figure(2-6-a).
2. Connect inputs A to SW1, D to SW2, outputs F4 to L1 (According to block C), then follow the input sequence and record the output F4 in table(2-6).

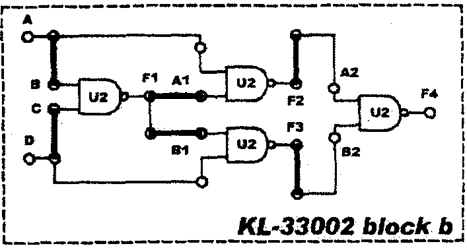


Fig.(2-6-a)

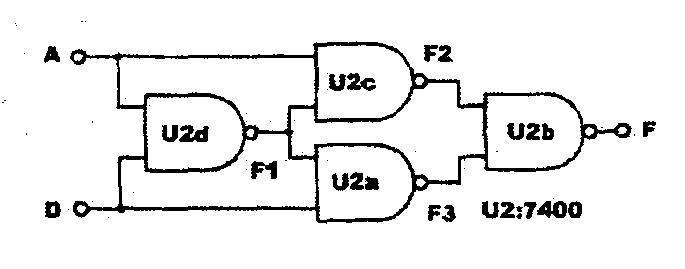


Fig.(2-6-b)

Table (2-6)

|  |  |  |
| --- | --- | --- |
| INPUT | | OUTPUT |
| SW1(D) | SW0(A) | F4 |
| 0 | 0 |  |
| 0 | 1 |  |
| 1 | 0 |  |
| 1 | 1 |  |

**Discussion:**

1. NOR gate can be used as:

**a. operational amplifier b. buffer c. Not**

2.What we get if connect A inputs short circuit in NOR gate?

**a. A b. Ā c. 0**

3. The output of NAND gate is equal to:

**a. + b. AB c. A+B**

4. Which of the following gates can be used to construct a XOR gate when there are four of them?

**a. OR. b. NOT. c. NAND.**

5. What we get if connect the inputs together in NAND gate?

6. What is the output if one input is logic '1' for a XOR gate?

7. Prove using Boolean algebra that the circuit drawn in figure (2-6-b) is an XOR gate.